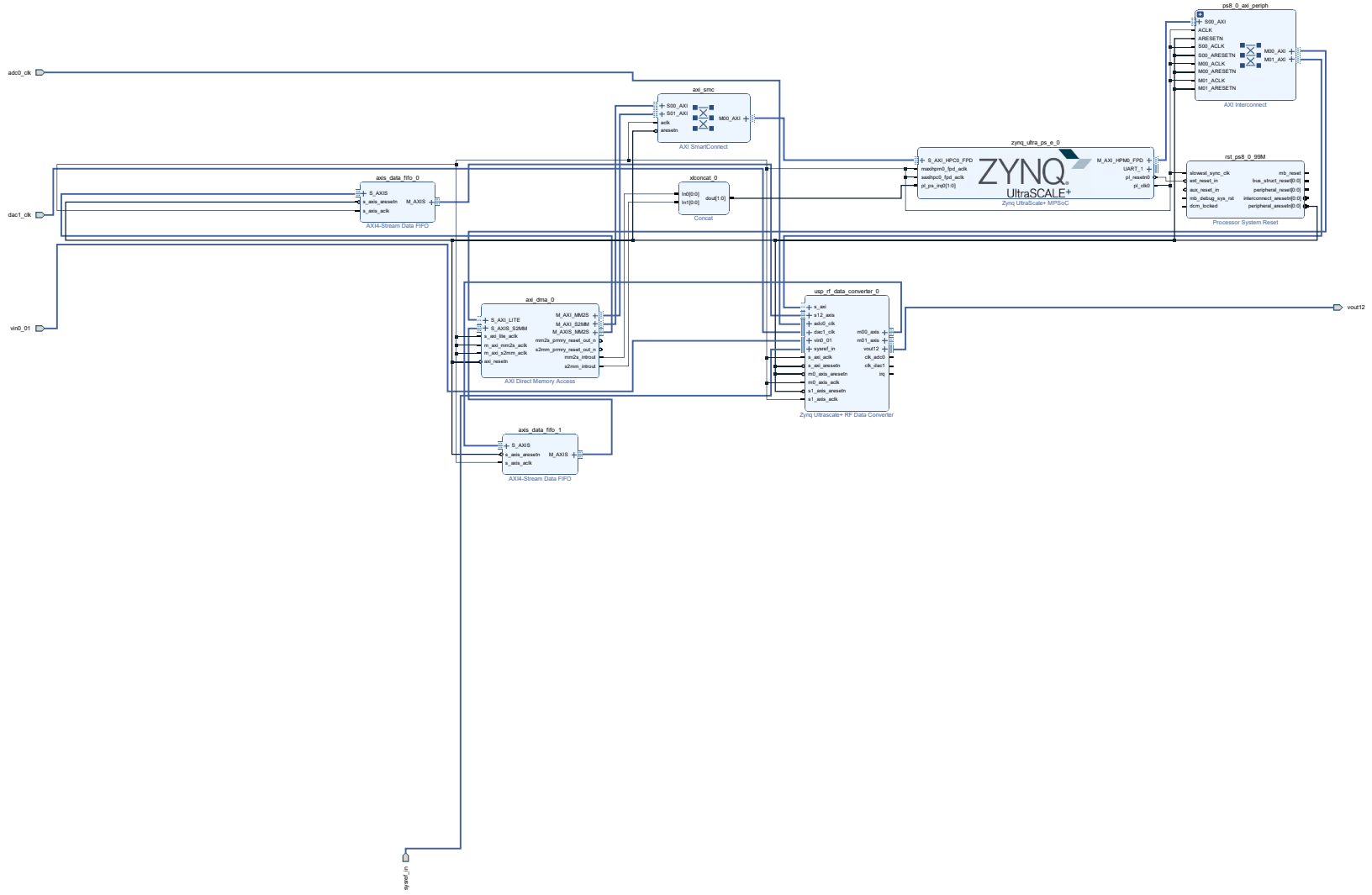
adc0_clk
dac1_clk
vin0_01
vout12
ps8_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
axi_smc
S00_AXI
S01_AXI
aclk
aresetn
M00_AXI
AXI SmartConnect
zynq_ultra_ps_e_0
S_AXI_HPC0_FPD
maxihpm0_fpd_aclk
saxihpc0_fpd_aclk
pl_ps_irq0[1:0]
M_AXI_HPM0_FPD
UART_1
pl_resetn0
pl_clk0
ZYNQ
UltraSCALE+
Zynq UltraScale+ MPSoC
rst_ps8_0_99M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axis_data_fifo_0
S_AXIS
s_axis_aresetn
s_axis_aclk
M_AXIS
AXI4-Stream Data FIFO
xlconcat_0
In0[0:0]
In1[0:0]
dout[1:0]
Concat
axi_dma_0
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_MM2S
M_AXI_S2MM
M_AXIS_MM2S
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
mm2s_introut
s2mm_introut
AXI Direct Memory Access
usp_rf_data_converter_0
s_axi
s12_axis
adc0_clk
dac1_clk
vin0_01
sysref_in
s_axi_aclk
s_axi_aresetn
m0_axis_aresetn
m0_axis_aclk
s1_axis_aresetn
s1_axis_aclk
m00_axis
m01_axis
vout12
clk_adc0
clk_dac1
irq
Zynq Ultrascale+ RF Data Converter
axis_data_fifo_1
S_AXIS
s_axis_aresetn
s_axis_aclk
M_AXIS
AXI4-Stream Data FIFO
irq_pulse