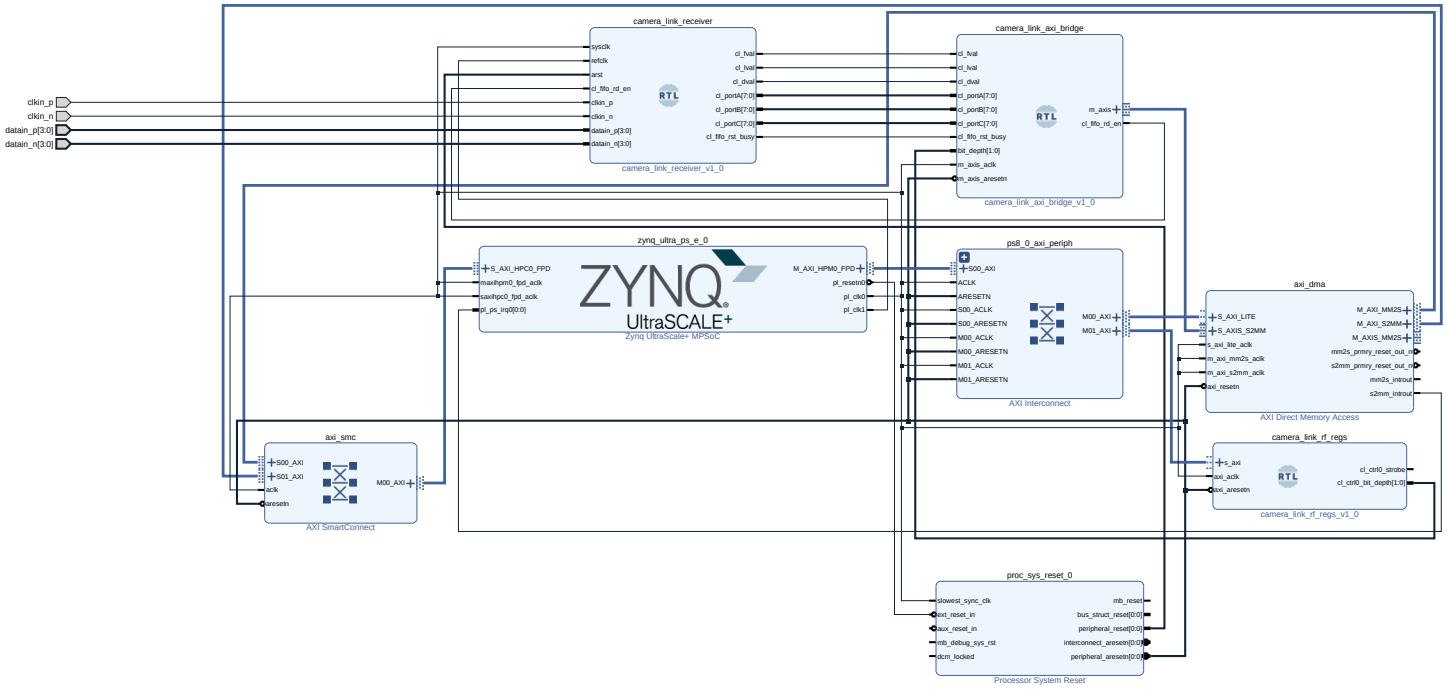
clkin_p
clkin_n
datain_p[3:0]
datain_n[3:0]
camera_link_receiver
sysclk
refclk
rst
cl_fifo_rd_en
clkin_p
clkin_n
datain_p[3:0]
datain_n[3:0]
cl_fval
cl_lval
cl_dval
cl_portA[7:0]
cl_portB[7:0]
cl_portC[7:0]
cl_fifo_rst_busy
camera_link_receiver_v1_0
camera_link_axi_bridge
cl_fval
cl_lval
cl_dval
cl_portA[7:0]
cl_portB[7:0]
cl_portC[7:0]
cl_fifo_rst_busy
bit_depth[1:0]
m_axis_aclk
m_axis_aresetn
m_axis
cl_fifo_rd_en
camera_link_axi_bridge_v1_0
zynq_ultra_ps_e_0
S_AXI_HPC0_FPD
maxihpm0_fpd_aclk
saxihpc0_fpd_aclk
pl_ps_irq0[0:0]
M_AXI_HPM0_FPD
pl_resetn0
pl_clk0
pl_clk1
ZYNQ
UltraSCALE+
Zynq UltraScale+ MPSoC
ps8_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
axi_dma
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_MM2S
M_AXI_S2MM
M_AXIS_MM2S
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
mm2s_introut
s2mm_introut
AXI Direct Memory Access
axi_smc
S00_AXI
S01_AXI
aclk
aresetn
M00_AXI
AXI SmartConnect
camera_link_rf_regs
s_axi
axi_aclk
axi_aresetn
cl_ctrl0_strobe
cl_ctrl0_bit_depth[1:0]
camera_link_rf_regs_v1_0
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset