

DMA Parameters

Width of Buffer Length Register (8-26) bits

Address Width (32-64) bits

Enable Read Channel

Number of Channels

Memory Map Data Width

Stream Data Width

Max Burst Size

Enable Write Channel

Number of Channels

Memory Map Data Width

Stream Data Width

Max Burst Size

Allow Unaligned Transfers

Allow Unaligned Transfers

ZYNQ ultrascale parameters:

slave ports:

Component Name

Basic	User Signals	Advanced
Protocol (Auto)	<input type="text" value="AXI4"/>	
Data Width (Auto)	<input type="text" value="64"/>	
Addr Width (Auto)	<input type="text" value="49"/>	[1 - 64]
Max Burst Length (Auto)	<input type="text" value="256"/>	[1 - 256]
Num Write Outstanding (Auto)	<input type="text" value="16"/>	[0 - 256]
Num Read Outstanding (Auto)	<input type="text" value="16"/>	[0 - 256]
Supports Narrow Burst (Auto)	<input type="text" value="0"/>	[0 - 1]
Id Width (Auto)	<input type="text" value="6"/>	
Read Write Mode (Auto)	<input type="text" value="READ WRITE"/>	
Frequency (MHz) (Auto)	<input type="text" value="99.999001"/>	
Clk Domain (Auto)	<input type="text" value="ltra_ps_e_0_0_pl_clk0"/>	
Phase (Auto)	<input type="text" value="0.000"/>	

Master Ports

Component Name

Basic	User Signals	Advanced
Protocol (Auto)	<input type="text" value="AXI4"/>	
Data Width (Auto)	<input type="text" value="32"/>	
Addr Width (Auto)	<input type="text" value="40"/>	[1 - 64]
Max Burst Length (Auto)	<input type="text" value="256"/>	[1 - 256]
Num Write Outstanding (Auto)	<input type="text" value="8"/>	[0 - 256]
Num Read Outstanding (Auto)	<input type="text" value="8"/>	[0 - 256]
Supports Narrow Burst (Auto)	<input type="text" value="1"/>	[0 - 1]
Id Width (Auto)	<input type="text" value="16"/>	
Read Write Mode (Auto)	<input type="text" value="READ WRITE"/>	
Frequency (MHz) (Auto)	<input type="text" value="99.999001"/>	
Clk Domain (Auto)	<input type="text" value="ltra_ps_e_0_0_pl_clk0"/>	
Phase (Auto)	<input type="text" value="0.000"/>	