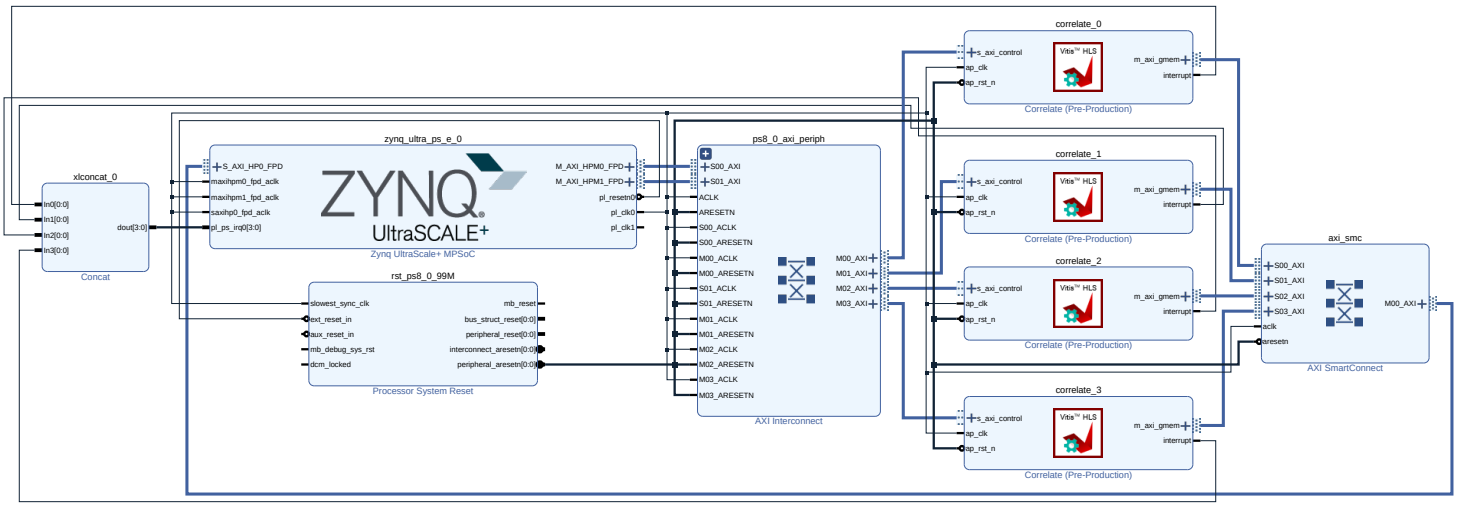
xlconcat_0
In0[0:0]
In1[0:0]
In2[0:0]
In3[0:0]
dout[3:0]
Concat
zynq_ultra_ps_e_0
S_AXI_HP0_FPD
maxihpm0_fpd_aclk
maxihpm1_fpd_aclk
saxihp0_fpd_aclk
pl_ps_irq0[3:0]
ZYNQ
UltraSCALE+
M_AXI_HPM0_FPD
M_AXI_HPM1_FPD
pl_resetn0
pl_clk0
pl_clk1
Zynq UltraScale+ MPSoC
rst_ps8_0_99M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
ps8_0_axi_periph
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
S01_ACLK
S01_ARESETN
M01_ACLK
M01_ARESETN
M02_ACLK
M02_ARESETN
M03_ACLK
M03_ARESETN
M00_AXI
M01_AXI
M02_AXI
M03_AXI
AXI Interconnect
correlate_0
s_axi_control
ap_clk
ap_rst_n
Vitis™ HLS
m_axi_gmem
interrupt
Correlate (Pre-Production)
correlate_1
correlate_2
correlate_3
axi_smc
S00_AXI
S01_AXI
S02_AXI
S03_AXI
aclk
aresetn
M00_AXI
AXI SmartConnect