Customize Pin

axi-stream (1.0)

Layered Metadata Summary

No Metadata defined

NOTE: Slave interfaces may not define
Metadata until Validation has been run

Component Name S_AXIS_S2MM

Signal Properties

Has Tlast (Auto)	true
Has Tkeep (Auto)	true
Has Tstrb (Auto)	false
Has Tready (Auto)	true
Tuser Width (Auto)	0
Tid Width (Auto)	0
Tdest Width (Auto)	0
Tdata Num Bytes (Auto)	4

Clock Properties

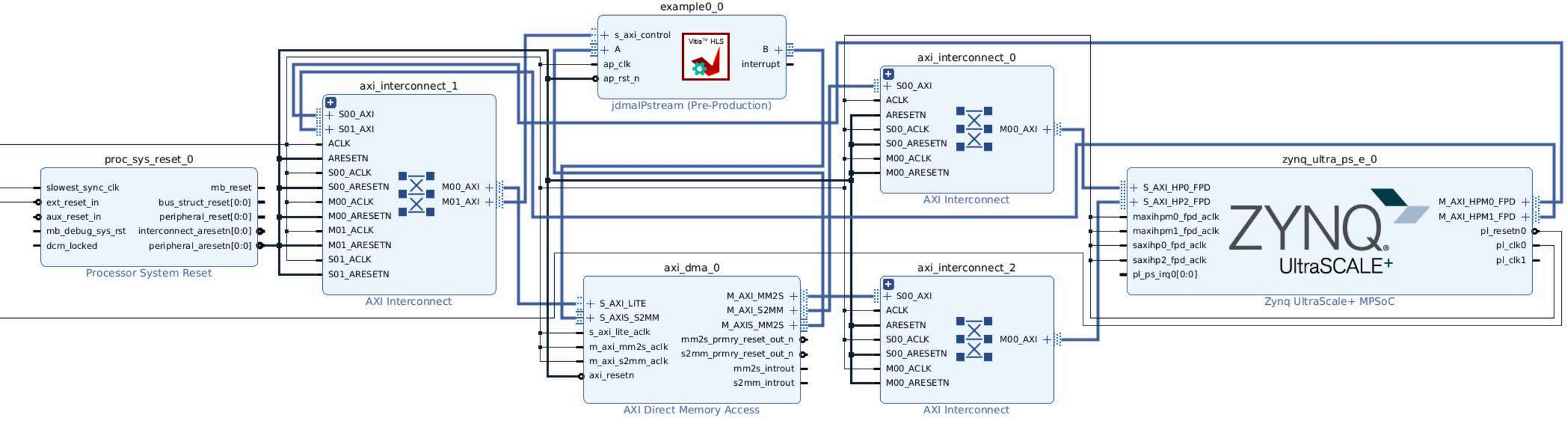
Clk Domain (Auto)	ltra_ps_e_0_1_pl_clk0
Phase (Auto)	0.0
Frequency (MHz) (Auto)	99.999001

Layered Data

Layered Metadata (Auto)	undef

OK

Cancel


example0_0
s_axi_control
A
ap_clk
ap_rst_n
B
interrupt
jdmaIPstream (Pre-Production)
axi_interconnect_1
S00_AXI
S01_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
S01_ACLK
S01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axi_interconnect_0
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
axi_dma_0
S_AXI_LITE
S_AXIS_S2MM
s_axi_lite_aclk
m_axi_mm2s_aclk
m_axi_s2mm_aclk
axi_resetn
M_AXI_MM2S
M_AXI_S2MM
M_AXIS_MM2S
mm2s_prmry_reset_out_n
s2mm_prmry_reset_out_n
mm2s_introut
s2mm_introut
AXI Direct Memory Access
axi_interconnect_2
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
zynq_ultra_ps_e_0
S_AXI_HP0_FPD
S_AXI_HP2_FPD
maxihpm0_fpd_aclk
maxihpm1_fpd_aclk
saxihp0_fpd_aclk
saxihp2_fpd_aclk
pl_ps_irq0[0:0]
M_AXI_HPM0_FPD
M_AXI_HPM1_FPD
pl_resetn0
pl_clk0
pl_clk1
Zynq UltraScale+ MPSoC

Copy the design files to the board

Rename and copy the BIT file and HWH file created by Vivado to a folder on your board. I renamed the files to:

- dma_axis_ip_example.bit
- dma_axis_ip_example.hwh

If you downloaded this notebook from GitHub you can also copy it notebook to the same folder. Alternatively, you can create a new Jupyter Notebook and copy the code into the new notebook to run it.

Instantiate and download the overlay

In [19]:
```
from pynq import Overlay

ol = Overlay("./dma_axis_ip_example.bit")
```

We can check the IPs in this overlay using the IP dictionary (*ip_dict*).

In [20]:
```
ol.ip_dict
```

Out[20]:

```
{'axi_dma_0': {'type': 'xilinx.com:ip:axi_dma:7.1',
  'mem_id': 'S_AXI_LITE',
  'memtype': 'REGISTER',
  'gpio': {},
  'interrupts': {},
  'parameters': {'C_S_AXI_LITE_ADDR_WIDTH': '10',
   'C_S_AXI_LITE_DATA_WIDTH': '32',
   'C_DLYTMR_RESOLUTION': '125',
   'C_PRMRY_IS_ACLK_ASYNC': '0',
   'C_ENABLE_MULTI_CHANNEL': '0',
   'C_NUM_MM2S_CHANNELS': '1',
   'C_NUM_S2MM_CHANNELS': '1',
   'C_INCLUDE_SG': '0',
   'C_SG_INCLUDE_STSCNTRL_STRM': '0',
   'C_SG_USE_STSAPP_LENGTH': '0',
   'C_SG_LENGTH_WIDTH': '26',
   'C_M_AXI_SG_ADDR_WIDTH': '32',
   'C_M_AXI_SG_DATA_WIDTH': '32',
   'C_M_AXIS_MM2S_CNTRL_TDATA_WIDTH': '32',
   'C_S_AXIS_S2MM_STS_TDATA_WIDTH': '32',
   'C_MICRO_DMA': '0',
   'C_INCLUDE_MM2S': '1',
   'C_INCLUDE_MM2S_SF': '1',
   'C_MM2S_BURST_SIZE': '16',
   'C_M_AXI_MM2S_ADDR_WIDTH': '32',
   'C_M_AXI_MM2S_DATA_WIDTH': '32',
   'C_M_AXIS_MM2S_TDATA_WIDTH': '32',
   'C_INCLUDE_MM2S_DRE': '0',
   'C_INCLUDE_S2MM': '1',
   'C_INCLUDE_S2MM_SF': '1',
   'C_S2MM_BURST_SIZE': '16',
   'C_M_AXI_S2MM_ADDR_WIDTH': '32',
   'C_M_AXI_S2MM_DATA_WIDTH': '32',
   'C_S_AXIS_S2MM_TDATA_WIDTH': '32',
   'C_INCLUDE_S2MM_DRE': '0',
   'C_INCREASE_THROUGHPUT': '0',
   'C_FAMILY': 'zynquplus',
   'Component_Name': 'design_1_axi_dma_0_0',
   'c_include_sg': '0',
   'c_enable_multi_channel': '0',
   'c_num_mm2s_channels': '1',
   'c_num_s2mm_channels': '1',
   'c_sg_length_width': '26',
   'c_dlytmr_resolution': '125',
   'c_prmry_is_aclk_async': '0',
   'c_sg_include_stscntrl_strm': '0',
   'c_micro_dma': '0',
   'c_include_mm2s': '1',
   'c_m_axi_mm2s_data_width': '32',
   'c_m_axis_mm2s_tdata_width': '32',
   'c_include_mm2s_dre': '0',
   'c_include_mm2s_sf': '1',
   'c_mm2s_burst_size': '16',
   'c_include_s2mm': '1',
   'c_sg_use_stsapp_length': '0',
   'c_m_axi_s2mm_data_width': '32',
   'c_s_axis_s2mm_tdata_width': '32',
   'c_include_s2mm_dre': '0',
   'c_include_s2mm_sf': '1',
   'c_s2mm_burst_size': '16',
   'c_addr_width': '32',
   'c_single_interface': '0',
   'c_increase_throughput': '0',
   'EDK_IPTYPE': 'PERIPHERAL',
   'C_BASEADDR': '0xA0000000',
   'C_HIGHADDR': '0xA000FFFF',
   'DATA_WIDTH': '32',
   'PROTOCOL': 'AXI4LITE',
   'FREQ_HZ': '99999001',
   'ID_WIDTH': '0',
   'ADDR_WIDTH': '10',
   'AWUSER_WIDTH': '0',
   'ARUSER_WIDTH': '0',
   'WUSER_WIDTH': '0',
   'RUSER_WIDTH': '0',
   'BUSER_WIDTH': '0',
   'READ_WRITE_MODE': 'READ_WRITE',
   'HAS_BURST': '0',
   'HAS_LOCK': '0',
   'HAS_PROT': '0',
   'HAS_CACHE': '0',
   'HAS_QOS': '0',
   'HAS_REGION': '0',
   'HAS_WSTRB': '0',
   'HAS_BRESP': '1',
   'HAS_RRESP': '1',
   'SUPPORTS_NARROW_BURST': '0',
   'NUM_READ_OUTSTANDING': '2',
   'NUM_WRITE_OUTSTANDING': '2',
   'MAX_BURST_LENGTH': '1',
   'PHASE': '0.0',
   'CLK_DOMAIN': 'design_1_zynq_ultra_ps_e_0_1_pl_clk0',
   'NUM_READ_THREADS': '1',
```

```
    'NUM_WRITE_THREADS': '1',
    'RUSER_BITS_PER_BYTE': '0',
    'WUSER_BITS_PER_BYTE': '0',
    'INSERT_VIP': '0',
    'TDATA_NUM_BYTES': '4',
    'TDEST_WIDTH': '0',
    'TID_WIDTH': '0',
    'TUSER_WIDTH': '0',
    'HAS_TREADY': '1',
    'HAS_TSTRB': '0',
    'HAS_TKEEP': '1',
    'HAS_TLAST': '1',
    'LAYERED_METADATA': 'undef'},
  'registers': {'MM2S_DMACR': {'address_offset': 0,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S DMA Control Register',
    'fields': {'RS': {'bit_offset': 0,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Run / Stop control for controlling running and stopping of the DMA channel.\n  0 - Stop - DMA s
tops when current (if any) DMA operations are complete. For Scatter / Gather Mode pending commands/transfers are flus
hed or completed. \n  AXI4-Stream outs are potentially terminated early. Descriptors in the update queue are allowed
to finish updating to remote memory before engine halt.\n  For Direct Register mode pending commands/transfers are fl
ushed or completed. AXI4-Stream outs are potentially terminated.\n  The halted bit in the DMA Status register asserts
to 1 when the DMA engine is halted. This bit is cleared by AXI DMA hardware when an error occurs. The CPU can also ch
oose to clear this bit to stop DMA operations.\n  1 - Run - Start DMA operations. The halted bit in the DMA Status re
gister deasserts to 0 when the DMA engine begins operations.\n'},
     'Reset': {'bit_offset': 2,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Soft reset for resetting the AXI DMA core. Setting this bit to a 1 causes the AXI DMA to be res
et. Reset is accomplished gracefully. Pending commands/transfers are flushed or completed.\nAXI4-Stream outs are pote
ntially terminated early. Setting either MM2S_DMACR. Reset = 1 or S2MM_DMACR.Reset = 1 resets the entire AXI DMA engi
ne. After completion of a soft reset, all registers and bits are in the Reset State.  0 - Normal operation.  1 -
Reset in progress.\n'},
     'Keyhole': {'bit_offset': 3,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Keyhole Read. Setting this bit to 1 causes AXI DMA to initiate MM2S reads (AXI4read) in non-inc
rementing address mode (Fixed Address Burst transfer on AXI4). This bit can be updated when AXI DMA is in idle. When
using keyhole operation the Max Burst Length should not exceed 16. This bit should not be set when DRE is enabled.\nT
his bit is non functional when the multichannel feature is enabled or in Direct Register mode.\n'},
     'Cyclic_BD_Enable': {'bit_offset': 4,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'When set to 1, the DMA operates in Cyclic Buffer Descriptor (BD) mode without any user interven
tion. In this mode, the Scatter Gather module ignores the Completed bit of the BD. With this bit set, you can use the
same BDs in cyclic manner without worrying about any stale descriptor errors.\nThis bit should be set/unset only when
the DMA is idle or when not running. Updating this bit while the DMA is running can result in unexpected behavior.\nT
his bit is non functional when DMA operates in multichannel mode.\n'},
     'IOC_IrqEn': {'bit_offset': 12,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Complete (IOC) Interrupt Enable. When set to 1, allows DMASR.IOC_Irq to generate a
n interrupt out for descriptors with the IOC bit set.  0 - IOC Interrupt disabled  1 - IOC Interrupt enabled
\n'},
     'Dly_IrqEn': {'bit_offset': 13,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Delay Timer Interrupt Enable. When set to 1, allows DMASR.Dly_Irq to generate an i
nterrupt out.  0 - Delay Interrupt disabled  1 - Delay Interrupt enabled Note: This field is ignored when AXI DM
A is configured for Direct Register Mode.\n'},
     'Err_IrqEn': {'bit_offset': 14,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Error Interrupt Enable.\n  0 - Error Interrupt disabled\n  1 - Error Interrupt ena
bled\n'},
     'IRQThreshold': {'bit_offset': 16,
      'bit_width': 8,
      'access': 'read-write',
      'description': 'Interrupt Threshold. This value is used for setting the interrupt threshold. When IOC interrupt
events occur, an internal counter counts down from the Interrupt Threshold setting. When the count reaches zero, an i
nterrupt out is generated by the DMA engine.  Note: The minimum setting for the threshold is 0x01. A write of 0x00 t
o this register has no effect.  Note: This field is ignored when AXI DMA is configured for Direct Register Mod
e.\n'},
     'IRQDelay': {'bit_offset': 24,
      'bit_width': 8,
      'access': 'read-write',
      'description': 'Interrupt Delay Time Out. This value is used for setting the interrupt timeout value. The inter
rupt timeout mechanism causes the DMA engine to generate an interrupt after the delay time period has expired. Timer
begins counting at the end of a packet and resets with receipt of a new packet or a timeout event occurs.\nNote: Sett
ing this value to zero disables the delay timer interrupt.\nNote: This field is ignored when AXI DMA is configured fo
r Direct Register Mode.\n'}}},
   'MM2S_DMASR': {'address_offset': 4,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S DMA Status Register',
    'fields': {'Halted': {'bit_offset': 0,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Channel Halted. Indicates the run/stop state of the DMA channel.  0 - DMA channel runni
ng.  1 - DMA channel halted.  For Scatter / Gather Mode this bit gets set when DMACR.RS = 0 and DMA and SG operat
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ions have halted. For Direct Register mode (C_INCLUDE_SG = 0) this bit gets set when DMACR.RS = 0 and DMA operations have halted. There can be a lag of time between when DMACR.RS = 0 and when DMASR.Halted = 1 Note: When halted (RS= 0 and Halted = 1), writing to CURDESC_PTR or TAILDESC_PTR pointer registers has no effect on DMA operations when in Sca tter Gather Mode. For Direct Register Mode, writing to the LENGTH register has no effect on DMA operations.\n'},
     'Idle': {'bit_offset': 1,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Channel Idle. Indicates the state of AXI DMA operations.\nFor Scatter / Gather Mode when ID LE indicates the SG Engine has reached the tail pointer for the associated channel and all queued descriptors have be en processed. Writing to the tail pointer register automatically restarts DMA operations.\nFor Direct Register Mode w hen IDLE indicates the current transfer has completed.      0 - Not Idle. For Scatter / Gather Mode, SG has not reach ed tail descriptor pointer and/or DMA operations in progress. For Direct Register Mode, transfer is not complete.
1 - Idle. For Scatter / Gather Mode, SG has reached tail descriptor pointer and DMA operation paused. for Direct Regi ster Mode, DMA transfer has completed and controller is paused.  Note: This bit is 0 when channel is halted (DMASR.Ha lted=1). This bit is also 0 prior to initial transfer when AXI DMA configured for Direct Register Mode.\n'},
     'SGIncld': {'bit_offset': 3,
      'bit_width': 1,
      'access': 'read-only',
      'description': '1 - Scatter Gather Enabled\n0 - Scatter Gather not enabled\n'},
     'DMAIntErr': {'bit_offset': 4,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Internal Error. Internal error occurs if the buffer length specified in the fetched descrip tor is set to 0. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when t he engine has completely shut down, the DMASR.Halted bit is set to 1.      0 - No DMA Internal Errors       1 - DMA Internal Error detected. DMA Engine halts\n'},
     'DMASlvErr': {'bit_offset': 5,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Slave Error. This error occurs if the slave read from the Memory Map interface issues a Sla ve Error. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when the engi ne has completely shut down, the DMASR.Halted bit is set to 1.      0 - No DMA Slave Errors.      1 - DMA Slave Error detected. DMA Engine halts\n'},
     'DMADecErr': {'bit_offset': 6,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Decode Error. This error occurs if the address request points to an invalid address. This e rror condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when the engine has completel y shut down, the DMASR.Halted bit is set to 1.      0 - No DMA Decode Errors.      1 - DMA Decode Error detected. DMA Engine halts.\n'},
     'SGIntErr': {'bit_offset': 8,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'Scatter Gather Internal Error. This error occurs if a descriptor with the “Complete bit” alread y set is fetched. Refer to the Scatter Gather Descriptor section for more information.This indicates to the SG Engine that the descriptor is a stale descriptor. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS b it is set to 0, and when the engine has completely shut down, the DMASR.Halted bit is set to 1.      0 - No SG Intern al Errors.      1 - SG Internal Error detected. DMA Engine halts.  Note: This bit is not used and is fixed at 0 when AXI DMA is configured for Direct Register Mode.\n'},
     'SGSlvErr': {'bit_offset': 9,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'Scatter Gather Slave Error. This error occurs if the slave read from on the Memory Map interfac e issues a Slave error. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when the engine has completely shut down, the DMASR.Halted bit is set to 1.      0 - No SG Slave Errors.      1 - SG Slave Error detected. DMA Engine halts.  Note: This bit is not used and is fixed at 0 when AXI DMA is configured for Direct Register Mode. \n'},
     'SGDecErr': {'bit_offset': 10,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'Scatter Gather Decode Error. This error occurs if CURDESC_PTR and/or NXTDESC_PTR points to an i nvalid address. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when th e engine has completely shut down, the DMASR.Halted bit is set to 1.      0 - No SG Decode Errors.      1 - SG Decode Error detected. DMA Engine halts.  Note: This bit is not used and is fixed at 0 when AXI DMA is configured for Direct Register Mode. \n'},
     'IOC_Irq': {'bit_offset': 12,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Complete. When set to 1 for Scatter/Gather Mode, indicates an interrupt event was generated on completion of a descriptor. This occurs for descriptors with the End of Frame (EOF) bit set. When set to 1 for Direct Register Mode, indicates an interrupt event was generated on completion of a transfer. If the correspond ing bit is enabled in the MM2S_DMACR (IOC_IrqEn = 1) and if the interrupt threshold has been met, causes an interrupt out to be generated from the AXI DMA.      0 - No IOC Interrupt.      1 - IOC Interrupt detected.  Writing a 1 to thi s bit will clear it.\n'},
     'Dly_Irq': {'bit_offset': 13,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Delay. When set to 1, indicates an interrupt event was generated on delay timer ti me out. If the corresponding bit is enabled in the MM2S_DMACR (Dly_IrqEn = 1), an interrupt out is generated from the AXI DMA.      0 - No Delay Interrupt.      1 - Delay Interrupt detected. Note: This bit is not used and is fixed at 0 when AXI DMA is configured for Direct Register Mode. \n'},
     'Err_Irq': {'bit_offset': 14,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Error. When set to 1, indicates an interrupt event was generated on error. If the corresponding bit is enabled in the MM2S_DMACR (Err_IrqEn = 1), an interrupt out is generated from the AXI DMA.\nWrit ing a 1 to this bit will clear it.   \n0 - No error Interrupt.   \n1 - Error interrupt detected.\n'},
     'IRQThresholdSts': {'bit_offset': 16,
      'bit_width': 8,
      'access': 'read-only',
      'description': 'Interrupt Threshold Status. Indicates current interrupt threshold value.\nNote: Applicable only when Scatter Gather is enabled.\n'},
     'IRQDelaySts': {'bit_offset': 24,
```

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      'bit_width': 8,
      'access': 'read-only',
      'description': 'Interrupt Delay Time Status. Indicates current interrupt delay time value.\nNote: Applicable on
ly when Scatter Gather is enabled.\n'}}},
   'MM2S_CURDESC': {'address_offset': 8,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S DMA Current Descriptor Pointer Register',
    'fields': {'Current_Descriptor_Pointer': {'bit_offset': 6,
      'bit_width': 26,
      'access': 'read-write',
      'description': 'Indicates the pointer of the current descriptor being worked on. This register must contain a p
ointer to a valid descriptor prior to writing the TAILDESC_PTR register. Otherwise, undefined results occur. When DMA
CR.RS is 1, CURDESC_PTR becomes Read Only (RO) and is used to fetch the first descriptor.\nWhen the DMA Engine is run
ning (DMACR.RS=1), CURDESC_PTR registers are updated by AXI DMA to indicate the current descriptor being worked on.\n
On error detection, CURDESC_PTR is updated to reflect the descriptor associated with the detected error.\nNote: The r
egister can only be written to by the CPU when the DMA Engine is Halted (DMACR.RS=0 and DMASR.Halted =1). At all othe
r times, this register is Read Only (RO). Descriptors must be 16 word aligned, that is, 0x00, 0x40, 0x80 and others.
Any other alignment has undefined results.\n'}}},
   'MM2S_CURDESC_MSB': {'address_offset': 12,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S DMA Current Descriptor Pointer Register',
    'fields': {'Current_Descriptor_Pointer': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the pointer of the current descriptor being worked on. This register must contain a p
ointer to a valid descriptor prior to writing the TAILDESC_PTR register. Otherwise, undefined results occur. When DMA
CR.RS is 1, CURDESC_PTR becomes Read Only (RO) and is used to fetch the first descriptor.\nWhen the DMA Engine is run
ning (DMACR.RS=1), CURDESC_PTR registers are updated by AXI DMA to indicate the current descriptor being worked on.\n
On error detection, CURDESC_PTR is updated to reflect the descriptor associated with the detected error.\nNote: The r
egister can only be written to by the CPU when the DMA Engine is Halted (DMACR.RS=0 and DMASR.Halted =1). At all othe
r times, this register is Read Only (RO). Descriptors must be 16 word aligned, that is, 0x00, 0x40, 0x80 and others.
Any other alignment has undefined results.\n'}}},
   'MM2S_TAILDESC': {'address_offset': 16,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S DMA Tail Descriptor Pointer Register',
    'fields': {'Tail_Descriptor_Pointer': {'bit_offset': 6,
      'bit_width': 26,
      'access': 'read-write',
      'description': 'Indicates the pause pointer in a descriptor chain. The AXI DMA SG Engine pauses descriptor fetc
hing after completing operations on the descriptor whose current descriptor pointer matches the tail descriptor point
er.\nWhen AXI DMA Channel is not halted (DMASR.Halted = 0), a write by the CPU to the TAILDESC_PTR register causes th
e AXI DMA SG Engine to start fetching descriptors or restart if it was idle (DMASR.Idle = 1). If it was not idle, wri
ting TAILDESC_PTR has no effect except to reposition the pause point.\nIf the AXI DMA Channel is halted (DMASR.Halted
= 1 and DMACR.RS = 0), a write by the CPU to the TAILDESC_PTR register has no effect except to reposition the pause p
oint.\nNote: The software must not move the tail pointer to a location that has not been updated. The software proces
ses and reallocates all completed descriptors (Cmplted = 1), clears the completed bits and then moves the tail pointe
r. The software must move the pointer to the last descriptor it updated. Descriptors must be 16-word aligned, that i
s, 0x00, 0x40, 0x80, and so forth. Any other alignment has undefined results. \n'}}},
   'MM2S_TAILDESC_MSB': {'address_offset': 20,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S DMA Tail Descriptor Pointer Register',
    'fields': {'Tail_Descriptor_Pointer': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the pause pointer in a descriptor chain. The AXI DMA SG Engine pauses descriptor fetc
hing after completing operations on the descriptor whose current descriptor pointer matches the tail descriptor point
er.\nWhen AXI DMA Channel is not halted (DMASR.Halted = 0), a write by the CPU to the TAILDESC_PTR register causes th
e AXI DMA SG Engine to start fetching descriptors or restart if it was idle (DMASR.Idle = 1). If it was not idle, wri
ting TAILDESC_PTR has no effect except to reposition the pause point.\nIf the AXI DMA Channel is halted (DMASR.Halted
= 1 and DMACR.RS = 0), a write by the CPU to the TAILDESC_PTR register has no effect except to reposition the pause p
oint.\nNote: The software must not move the tail pointer to a location that has not been updated. The software proces
ses and reallocates all completed descriptors (Cmplted = 1), clears the completed bits and then moves the tail pointe
r. The software must move the pointer to the last descriptor it updated. Descriptors must be 16-word aligned, that i
s, 0x00, 0x40, 0x80, and so forth. Any other alignment has undefined results. \n'}}},
   'MM2S_SA': {'address_offset': 24,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S Source Address Register',
    'fields': {'Source_Address': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the source address AXI DMA reads from to transfer data to AXI4-Stream on the MM2S Cha
nnel.\nNote: If Data Realignment Engine is included, the Source Address can be at any byte offset. If Data Realignmen
t Engine is not included, the Source Address must be MM2S Memory Map data width aligned.\n'}}},
   'MM2S_SA_MSB': {'address_offset': 28,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S Source Address Register',
    'fields': {'Source_Address': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the MSB 32 bits of the source address AXI DMA reads from to transfer data to AXI4-Str
eam on the MM2S Channel.\nNote: If Data Realignment Engine is included, the Source Address can be at any byte offset.
If Data Realignment Engine is not included, the Source Address must be MM2S Memory Map data width aligned.\n'}}},
   'MM2S_LENGTH': {'address_offset': 40,
    'size': 32,
    'access': 'read-write',
    'description': 'MM2S DMA Transfer Length Register',
    'fields': {'Length': {'bit_offset': 0,
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      'bit_width': 26,
      'access': 'read-write',
      'description': 'Indicates the number of bytes to transfer for the MM2S channel. Writing a non-zero value to thi
s register starts the MM2S transfer.\n'}},
   'SG_CTL': {'address_offset': 44,
    'size': 32,
    'access': 'read-write',
    'description': 'Scatter/Gather User and Cache Control Register',
    'fields': {'SG_CACHE': {'bit_offset': 0,
      'bit_width': 4,
      'access': 'read-write',
      'description': 'Scatter/Gather Cache Control. Values written in this register reflect on the m_axi_sg_arcache a
nd m_axi_sg_awcache signals of the M_AXI_SG interface.\n'},
     'SG_USER': {'bit_offset': 8,
      'bit_width': 4,
      'access': 'read-write',
      'description': 'Scatter/Gather User Control. Values written in this register reflect on the m_axi_sg_aruser and
m_axi_sg_awuser signals of the M_AXI_SG interface.\n'}}},
   'S2MM_DMACR': {'address_offset': 48,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM DMA Control Register',
    'fields': {'RS': {'bit_offset': 0,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Run / Stop control for controlling running and stopping of the DMA channel.\n  0 - Stop - DMA s
tops when current (if any) DMA operations are complete. For Scatter / Gather Mode pending commands/transfers are flus
hed or completed. \n  AXI4-Stream outs are potentially terminated early. Descriptors in the update queue are allowed
to finish updating to remote memory before engine halt.\n  For Direct Register mode pending commands/transfers are fl
ushed or completed. AXI4-Stream outs are potentially terminated. Data integrity on S2MM AXI4 cannot be guaranteed.\n
The halted bit in the DMA Status register asserts to 1 when the DMA engine is halted. This bit is cleared by AXI DMA
hardware when an error occurs. The CPU can also choose to clear this bit to stop DMA operations.\n  1 - Run - Start D
MA operations. The halted bit in the DMA Status register deasserts to 0 when the DMA engine begins operations.\n'},
     'Reset': {'bit_offset': 2,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Soft reset for resetting the AXI DMA core. Setting this bit to a 1 causes the AXI DMA to be res
et. Reset is accomplished gracefully. Pending commands/transfers are flushed or completed.\nAXI4-Stream outs are term
inated early, if necessary with associated TLAST. Setting either MM2S_DMACR.Reset = 1 or S2MM_DMACR.Reset = 1 resets
the entire AXI DMA engine. After completion of a soft reset, all registers and bits are in the Reset State.      0 -
Reset not in progress. Normal operation.      1 - Reset in progress\n'},
     'Keyhole': {'bit_offset': 3,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Keyhole Write. Setting this bit to 1 causes AXI DMA to initiate S2MM writes (AXI4 Writes) in no
n-incrementing address mode (Fixed Address Burst transfer on AXI4). This bit can be modified when AXI DMA is in idle.
When enabling Key hole operation the maximum burst length cannot be more than 16. This bit should not be set when DRE
is enabled.\nThis bit is non functional when DMA is used in multichannel mode.\n'},
     'Cyclic_BD_Enable': {'bit_offset': 4,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'When set to 1, the DMA operates in Cyclic Buffer Descriptor (BD) mode without any user interven
tion. In this mode, the Scatter Gather module ignores the Completed bit of the BD. With this bit set, you can use the
same BDs in cyclic manner without worrying about any stale descriptor errors.\nThis bit is non functional when DMA op
erates in Multichannel mode. or in Direct Register Mode\n'},
     'IOC_IrqEn': {'bit_offset': 12,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Complete (IOC) Interrupt Enable. When set to 1, allows Interrupt On Complete event
s to generate an interrupt out for descriptors with the Complete bit set.      0 - IOC Interrupt disabled      1 - IO
C Interrupt enabled\n'},
     'Dly_IrqEn': {'bit_offset': 13,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Delay Timer Interrupt Enable. When set to 1, allows error events to generate an in
terrupt out.      0 - Delay Interrupt disabled      1 - Delay Interrupt enabled  Note: Applicable only when Scatter G
ather is enabled.\n'},
     'Err_IrqEn': {'bit_offset': 14,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Error Interrupt Enable. When set to 1, allows error events to generate an interrup
t out.      0 - Error Interrupt disabled      1 - Error Interrupt enabled\n'},
     'IRQThreshold': {'bit_offset': 16,
      'bit_width': 8,
      'access': 'read-write',
      'description': 'Interrupt Threshold. This value is used for setting the interrupt threshold. When IOC interrupt
events occur, an internal counter counts down from the Interrupt Threshold setting. When the count reaches zero, an i
nterrupt out is generated by the DMA engine.\nNote: The minimum setting for the threshold is 0x01. A write of 0x00 to
this register has no effect.\nNote: Applicable only when Scatter Gather is enabled.\n'},
     'IRQDelay': {'bit_offset': 24,
      'bit_width': 8,
      'access': 'read-write',
      'description': 'Interrupt Delay Time Out. This value is used for setting the interrupt timeout value. The inter
rupt timeout mechanism causes the DMA engine to generate an interrupt after the delay time period has expired. Timer
begins counting at the end of a packet and resets with receipt of a new packet or a timeout event occurs.\nNote: Sett
ing this value to zero disables the delay timer interrupt.\nNote: Applicable only when Scatter Gather is enable
d.\n'}}},
   'S2MM_DMASR': {'address_offset': 52,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM DMA Status Register',
    'fields': {'Halted': {'bit_offset': 0,
      'bit_width': 1,
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      'access': 'read-only',
      'description': 'DMA Channel Halted. Indicates the run/stop state of the DMA channel.      0 - DMA channel runni
ng.      1 - DMA channel halted.  For Scatter/Gather Mode this bit gets set when DMACR.RS = 0 and DMA and SG operatio
ns have halted. For Direct Register Mode this bit gets set when DMACR.RS = 0 and DMA operations have halted. There ca
n be a lag of time between when DMACR.RS = 0 and when DMASR.Halted = 1 \nNote: When halted (RS= 0 and Halted = 1), wr
iting to CURDESC_PTR or TAILDESC_PTR pointer registers has no effect on DMA operations when in Scatter Gather Mode. F
or Direct Register Mode, writing to the LENGTH register has no effect on DMA operations.\n'},
     'Idle': {'bit_offset': 1,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Channel Idle. Indicates the state of AXI DMA operations.\nFor Scatter / Gather Mode when ID
LE indicates the SG Engine has reached the tail pointer for the associated channel and all queued descriptors have be
en processed. Writing to the tail pointer register automatically restarts DMA operations.\nFor Direct Register Mode w
hen IDLE indicates the current transfer has completed.      0 - Not Idle.      1 - Idle.   Note: This bit is 0 when c
hannel is halted (DMASR.Halted=1). This bit is also 0 prior to initial transfer when AXI DMA configured for Direct Re
gister Mode.\n'},
     'SGIncld': {'bit_offset': 3,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'Scatter Gather Engine Included. DMASR.SGIncld = 1 indicates the Scatter Gather engine is includ
ed and the AXI DMA is configured for Scatter Gather mode. DMASR.SGIncld = 0 indicates the Scatter Gather engine is ex
cluded and the AXI DMA is configured for Direct Register Mode.\n'},
     'DMAIntErr': {'bit_offset': 4,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Internal Error. This error occurs if the buffer length specified in the fetched descriptor
is set to 0. Also, when in Scatter Gather Mode and using the status app length field, this error occurs when the Stat
us AXI4-Stream packet RxLength field does not match the S2MM packet being received by the S_AXIS_S2MM interface. When
Scatter Gather is disabled, this error is flagged if any error occurs during Memory write or if the incoming packet i
s bigger than what is specified in the DMA length register.\nThis error condition causes the AXI DMA to halt graceful
ly. The DMACR.RS bit is set to 0, and when the engine has completely shut down, the DMASR.Halted bit is set to 1.
0 - No DMA Internal Errors      1 - DMA Internal Error detected.\n'},
     'DMASlvErr': {'bit_offset': 5,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Slave Error. This error occurs if the slave read from the Memory Map interface issues a Sla
ve Error. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when the engi
ne has completely shut down, the DMASR.Halted bit is set to 1.      0 - No DMA Slave Errors.      1 - DMA Slave Error
detected.\n'},
     'DMADecErr': {'bit_offset': 6,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'DMA Decode Error. This error occurs if the address request points to an invalid address. This e
rror condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when the engine has completel
y shut down, the DMASR.Halted bit is set to 1.     0 - No DMA Decode Errors.   1 - DMA Decode Error detected.\n'},
     'SGIntErr': {'bit_offset': 8,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'Scatter Gather Internal Error. This error occurs if a descriptor with the “Complete bit” alread
y set is fetched. This indicates to the SG Engine that the descriptor is a tail descriptor. This error condition caus
es the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when the engine has completely shut down, the DM
ASR.Halted bit is set to 1.      0 - No SG Internal Errors.      1 - SG Internal Error detected.  Note: Applicable on
ly when Scatter Gather is enabled. \n'},
     'SGSlvErr': {'bit_offset': 9,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'Scatter Gather Slave Error. This error occurs if the slave read from on the Memory Map interfac
e issues a Slave error. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and
when the engine has completely shut down, the DMASR.Halted bit is set to 1.      0 - No SG Slave Errors.      1 - SG
Slave Error detected. DMA Engine halts. Note: Applicable only when Scatter Gather is enabled. \n'},
     'SGDecErr': {'bit_offset': 10,
      'bit_width': 1,
      'access': 'read-only',
      'description': 'Scatter Gather Decode Error. This error occurs if CURDESC_PTR and/or NXTDESC_PTR points to an i
nvalid address. This error condition causes the AXI DMA to halt gracefully. The DMACR.RS bit is set to 0, and when th
e engine has completely shut down, the DMASR.Halted bit is set to 1.      0 - No SG Decode Errors.      1 - SG Decode
Error detected. DMA Engine halts. Note: Applicable only when Scatter Gather is enabled. \n'},
     'IOC_Irq': {'bit_offset': 12,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Complete. When set to 1 for Scatter/Gather Mode, indicates an interrupt event was
generated on completion of a descriptor. This occurs for descriptors with the End of Frame (EOF) bit set. When set to
1 for Direct Register Mode, indicates an interrupt event was generated on completion of a transfer. If the correspond
ing bit in S2MM_DMACR is enabled (IOC_IrqEn = 1) and if the interrupt threshold has been met, causes an interrupt out
to be generated from the AXI DMA.      0 - No IOC Interrupt.      1 - IOC Interrupt detected. Writing a 1 to this bit
will clear it.\n'},
     'Dly_Irq': {'bit_offset': 13,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Delay. When set to 1, indicates an interrupt event was generated on delay timer ti
me out. If the corresponding bit is enabled in the S2MM_DMACR (Dly_IrqEn = 1), an interrupt out is generated from the
AXI DMA.      0 - No Delay Interrupt.      1 - Delay Interrupt detected.1 = IOC Interrupt detected. Writing a 1 to th
is bit will clear it. Note: Applicable only when Scatter Gather is enabled. \n'},
     'Err_Irq': {'bit_offset': 14,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Interrupt on Error. When set to 1, indicates an interrupt event was generated on error. If the
corresponding bit is enabled in the S2MM_DMACR (Err_IrqEn = 1), an interrupt out is generated from the AXI DMA.\nWrit
ing a 1 to this bit will clear it.      0 - No error Interrupt.      1 - Error interrupt detected.\n'},
     'IRQThresholdSts': {'bit_offset': 16,
      'bit_width': 8,
      'access': 'read-only',
      'description': 'Interrupt Threshold Status. Indicates current interrupt threshold value.\nNote: Applicable only
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when Scatter Gather is enabled.\n'},
     'IRQDelaySts': {'bit_offset': 24,
      'bit_width': 8,
      'access': 'read-only',
      'description': 'Interrupt Delay Time Status. Indicates current interrupt delay time value.\nNote: Applicable on
ly when Scatter Gather is enabled.\n'}}},
   'S2MM_CURDESC': {'address_offset': 56,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM DMA Current Descriptor Pointer Register',
    'fields': {'Current_Descriptor_Pointer': {'bit_offset': 6,
      'bit_width': 26,
      'access': 'read-write',
      'description': 'Indicates the pointer of the current descriptor being worked on. This register must contain a p
ointer to a valid descriptor prior to writing the TAILDESC_PTR register. Otherwise, undefined results occur. When DMA
CR.RS is 1, CURDESC_PTR becomes Read Only (RO) and is used to fetch the first descriptor.\nWhen the DMA Engine is run
ning (DMACR.RS=1), CURDESC_PTR registers are updated by AXI DMA to indicate the current descriptor being worked on.\n
On error detection, CURDESC_PTR is updated to reflect the descriptor associated with the detected error.\nNote: The r
egister can only be written to by the CPU when the DMA Engine is Halted (DMACR.RS=0 and DMASR.Halted =1). At all othe
r times, this register is Read Only (RO). \nBuffer Descriptors must be 16 word aligned, that is, 0x00, 0x40, 0x80 and
so forth. Any other alignment has undefined results.\n'}}},
   'S2MM_CURDESC_MSB': {'address_offset': 60,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM DMA Current Descriptor Pointer Register',
    'fields': {'Current_Descriptor_Pointer': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the pointer of the current descriptor being worked on. This register must contain a p
ointer to a valid descriptor prior to writing the TAILDESC_PTR register. Otherwise, undefined results occur. When DMA
CR.RS is 1, CURDESC_PTR becomes Read Only (RO) and is used to fetch the first descriptor.\nWhen the DMA Engine is run
ning (DMACR.RS=1), CURDESC_PTR registers are updated by AXI DMA to indicate the current descriptor being worked on.\n
On error detection, CURDESC_PTR is updated to reflect the descriptor associated with the detected error.\nNote: The r
egister can only be written to by the CPU when the DMA Engine is Halted (DMACR.RS=0 and DMASR.Halted =1). At all othe
r times, this register is Read Only (RO). Descriptors must be 16 word aligned, that is, 0x00, 0x40, 0x80 and others.
Any other alignment has undefined results.\n'}}},
   'S2MM_TAILDESC': {'address_offset': 64,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM DMA Tail Descriptor Pointer Register',
    'fields': {'Tail_Descriptor_Pointer': {'bit_offset': 6,
      'bit_width': 26,
      'access': 'read-write',
      'description': 'Indicates the pause pointer in a descriptor chain. The AXI DMA SG Engine pauses descriptor fetc
hing after completing operations on the descriptor whose current descriptor pointer matches the tail descriptor point
er.\nWhen AXI DMA Channel is not halted (DMASR.Halted = 0), a write by the CPU to the TAILDESC_PTR register causes th
e AXI DMA SG Engine to start fetching descriptors or restart if it was idle (DMASR.Idle = 1). If it was not idle, wri
ting TAILDESC_PTR has no effect except to reposition the pause point.\nIf the AXI DMA Channel DMACR.RS bit is set to
0 (DMASR.Halted = 1 and DMACR.RS = 0), a write by the CPU to the TAILDESC_PTR register has no effect except to reposi
tion the pause point.\nNote: The software must not move the tail pointer to a location that has not been updated. The
software processes and reallocates all completed descriptors (Cmplted = 1), clears the completed bits and then moves
the tail pointer. The software must move the pointer to the last descriptor it updated. \nDescriptors must be 16-word
aligned, that is, 0x00, 0x40, 0x80, and so forth. Any other alignment has undefined results. \n'}}},
   'S2MM_TAILDESC_MSB': {'address_offset': 68,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM DMA Tail Descriptor Pointer Register',
    'fields': {'Tail_Descriptor_Pointer': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the pause pointer in a descriptor chain. The AXI DMA SG Engine pauses descriptor fetc
hing after completing operations on the descriptor whose current descriptor pointer matches the tail descriptor point
er.\nWhen AXI DMA Channel is not halted (DMASR.Halted = 0), a write by the CPU to the TAILDESC_PTR register causes th
e AXI DMA SG Engine to start fetching descriptors or restart if it was idle (DMASR.Idle = 1). If it was not idle, wri
ting TAILDESC_PTR has no effect except to reposition the pause point.\nIf the AXI DMA Channel is halted (DMASR.Halted
= 1 and DMACR.RS = 0), a write by the CPU to the TAILDESC_PTR register has no effect except to reposition the pause p
oint.\nNote: The software must not move the tail pointer to a location that has not been updated. The software proces
ses and reallocates all completed descriptors (Cmplted = 1), clears the completed bits and then moves the tail pointe
r. The software must move the pointer to the last descriptor it updated. Descriptors must be 16-word aligned, that i
s, 0x00, 0x40, 0x80, and so forth. Any other alignment has undefined results. \n'}}},
   'S2MM_DA': {'address_offset': 72,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM DMA Destination Address Register',
    'fields': {'Destination_Address': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the destination address the AXI DMA writes to transfer data from AXI4-Stream on S2MM
Channel.\nNote: If Data Realignment Engine is included, the Destination Address can be at any byte offset. If Data Re
alignment Engine is not included, the Destination Address must be S2MM Memory Map data width aligned.\n'}}},
   'S2MM_DA_MSB': {'address_offset': 76,
    'size': 32,
    'access': 'read-write',
    'description': 'S2MM Destination Address Register',
    'fields': {'Destination_Address': {'bit_offset': 0,
      'bit_width': 32,
      'access': 'read-write',
      'description': 'Indicates the MSB 32 bits of the Destination address AXI DMA writes to transfer data from AXI4-
Stream on the S2MM Channel.\nNote: If Data Realignment Engine is included, the Destination Address can be at any byte
offset. If Data Realignment Engine is not included, the Dstination Address must be S2MM Memory Map data width aligne
d.\n'}}},
   'S2MM_LENGTH': {'address_offset': 88,
    'size': 32,
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    'access': 'read-write',
    'description': 'S2MM DMA Transfer Length Register',
    'fields': {'Length': {'bit_offset': 0,
      'bit_width': 26,
      'access': 'read-write',
      'description': 'Indicates the length in bytes of the S2MM buffer available to write receive data from the S2MM
channel. Writing a non-zero value to this register enables S2MM channel to receive packet data.\nAt the completion of
the S2MM transfer, the number of actual bytes written on the S2MM AXI4 interface is updated to the S2MM_LENGTH regist
er.\nNote: This value must be greater than or equal to the largest expected packet to be received on S2MM AXI4-Strea
m. Values smaller than the received packet result in undefined behavior. \n'}}}},
  'driver': pynq.lib.dma.DMA,
  'device': <pynq.pl_server.embedded_device.EmbeddedDevice at 0xffffb39cfa60>,
  'state': None,
  'bdtype': None,
  'phys_addr': 2684354560,
  'addr_range': 65536,
  'fullpath': 'axi_dma_0'},
 'example0_0': {'type': 'jie:hls:example0:1.0',
  'mem_id': 's_axi_control',
  'memtype': 'REGISTER',
  'gpio': {},
  'interrupts': {},
  'parameters': {'C_S_AXI_CONTROL_ADDR_WIDTH': '4',
   'C_S_AXI_CONTROL_DATA_WIDTH': '32',
   'Component_Name': 'design_1_example0_0_1',
   'clk_period': '10',
   'machine': '64',
   'combinational': '0',
   'latency': 'undef',
   'II': 'x',
  'EDK_IPTYPE': 'PERIPHERAL',
  'C_S_AXI_CONTROL_BASEADDR': '0xB0000000',
  'C_S_AXI_CONTROL_HIGHADDR': '0xB000FFFF',
  'ADDR_WIDTH': '4',
  'DATA_WIDTH': '32',
  'PROTOCOL': 'AXI4LITE',
  'READ_WRITE_MODE': 'READ_WRITE',
  'FREQ_HZ': '99999001',
  'ID_WIDTH': '0',
  'AWUSER_WIDTH': '0',
  'ARUSER_WIDTH': '0',
  'WUSER_WIDTH': '0',
  'RUSER_WIDTH': '0',
  'BUSER_WIDTH': '0',
  'HAS_BURST': '0',
  'HAS_LOCK': '0',
  'HAS_PROT': '0',
  'HAS_CACHE': '0',
  'HAS_QOS': '0',
  'HAS_REGION': '0',
  'HAS_WSTRB': '1',
  'HAS_BRESP': '1',
  'HAS_RRESP': '1',
  'SUPPORTS_NARROW_BURST': '0',
  'NUM_READ_OUTSTANDING': '1',
  'NUM_WRITE_OUTSTANDING': '1',
  'MAX_BURST_LENGTH': '1',
  'PHASE': '0.0',
  'CLK_DOMAIN': 'design_1_zynq_ultra_ps_e_0_1_pl_clk0',
  'NUM_READ_THREADS': '1',
  'NUM_WRITE_THREADS': '1',
  'RUSER_BITS_PER_BYTE': '0',
  'WUSER_BITS_PER_BYTE': '0',
  'INSERT_VIP': '0',
  'TDATA_NUM_BYTES': '4',
  'TDEST_WIDTH': '6',
  'TID_WIDTH': '5',
  'TUSER_WIDTH': '2',
  'LAYERED_METADATA': None,
  'HAS_TREADY': '1',
  'HAS_TSTRB': '1',
  'HAS_TKEEP': '1',
  'HAS_TLAST': '1'},
 'registers': {'CTRL': {'address_offset': 0,
   'size': 32,
   'access': 'read-write',
   'description': 'Control signals',
   'fields': {'AP_START': {'bit_offset': 0,
     'bit_width': 1,
     'access': 'read-write',
     'description': "Control signal Register for 'ap_start'."},
    'AP_DONE': {'bit_offset': 1,
     'bit_width': 1,
     'access': 'read-only',
     'description': "Control signal Register for 'ap_done'."},
    'AP_IDLE': {'bit_offset': 2,
     'bit_width': 1,
     'access': 'read-only',
     'description': "Control signal Register for 'ap_idle'."},
    'AP_READY': {'bit_offset': 3,
     'bit_width': 1,
     'access': 'read-only',
     'description': "Control signal Register for 'ap_ready'."},
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      'RESERVED_1': {'bit_offset': 4,
       'bit_width': 3,
       'access': 'read-only',
       'description': 'Reserved.  0s on read.'},
      'AUTO_RESTART': {'bit_offset': 7,
       'bit_width': 1,
       'access': 'read-write',
       'description': "Control signal Register for 'auto_restart'."},
      'RESERVED_2': {'bit_offset': 8,
       'bit_width': 1,
       'access': 'read-only',
       'description': 'Reserved.  0s on read.'},
      'INTERRUPT': {'bit_offset': 9,
       'bit_width': 1,
       'access': 'read-only',
       'description': "Control signal Register for 'interrupt'."},
      'RESERVED_3': {'bit_offset': 10,
       'bit_width': 22,
       'access': 'read-only',
       'description': 'Reserved.  0s on read.'}}},
   'GIER': {'address_offset': 4,
    'size': 32,
    'access': 'read-write',
    'description': 'Global Interrupt Enable Register',
    'fields': {'Enable': {'bit_offset': 0,
      'bit_width': 1,
      'access': 'read-write',
      'description': 'Master enable for the device interrupt output to the system interrupt controller: 0 = Disabled,
1 = Enabled'},
     'RESERVED': {'bit_offset': 1,
      'bit_width': 31,
      'access': 'read-only',
      'description': 'Reserved.  0s on read.'}}},
  'IP_IER': {'address_offset': 8,
   'size': 32,
   'access': 'read-write',
   'description': 'IP Interrupt Enable Register',
   'fields': {'CHAN0_INT_EN': {'bit_offset': 0,
     'bit_width': 1,
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o0[23]#scl_out#sda_out#gpi[0]#gpio1[27]#gpio1[28]#gpio1[29]#gpio1[30]#gpi[5]#gpo[0]#gpo[1]#gpo[2]#gpo[3]#gpio1[36]#gp
io1[37]#gpio1[38]#gpio1[39]#gpio1[40]#gpio1[41]#gpio1[42]#gpio1[43]#gpio1[44]#gpio1[45]#gpio1[46]#gpio1[47]#gpio1[48]
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                'PSU_MIO_38_DRIVE_STRENGTH': '4',
                'PSU_MIO_38_POLARITY': 'Default',
                'PSU_MIO_38_INPUT_TYPE': 'cmos',
                'PSU_MIO_38_SLEW': 'slow',
                'PSU_MIO_38_DIRECTION': 'inout',
                'PSU_MIO_39_PULLUPDOWN': 'pullup',
                'PSU_MIO_39_DRIVE_STRENGTH': '4',
                'PSU_MIO_39_POLARITY': 'Default',
                'PSU_MIO_39_INPUT_TYPE': 'cmos',
                'PSU_MIO_39_SLEW': 'slow',
                'PSU_MIO_39_DIRECTION': 'inout',
                'PSU_MIO_40_PULLUPDOWN': 'pullup',
                'PSU_MIO_40_DRIVE_STRENGTH': '4',
                'PSU_MIO_40_POLARITY': 'Default',
                'PSU_MIO_40_INPUT_TYPE': 'cmos',
                'PSU_MIO_40_SLEW': 'slow',
                'PSU_MIO_40_DIRECTION': 'inout',
                'PSU_MIO_41_PULLUPDOWN': 'pullup',
                'PSU_MIO_41_DRIVE_STRENGTH': '4',
                'PSU_MIO_41_POLARITY': 'Default',
                'PSU_MIO_41_INPUT_TYPE': 'cmos',
                'PSU_MIO_41_SLEW': 'slow',
                'PSU_MIO_41_DIRECTION': 'inout',
                'PSU_MIO_42_PULLUPDOWN': 'pullup',
                'PSU_MIO_42_DRIVE_STRENGTH': '4',
                'PSU_MIO_42_POLARITY': 'Default',
                'PSU_MIO_42_INPUT_TYPE': 'cmos',
                'PSU_MIO_42_SLEW': 'slow',
                'PSU_MIO_42_DIRECTION': 'inout',
                'PSU_MIO_43_PULLUPDOWN': 'pullup',
                'PSU_MIO_43_DRIVE_STRENGTH': '4',
                'PSU_MIO_43_POLARITY': 'Default',
                'PSU_MIO_43_INPUT_TYPE': 'cmos',
                'PSU_MIO_43_SLEW': 'slow',
                'PSU_MIO_43_DIRECTION': 'inout',
                'PSU_MIO_44_PULLUPDOWN': 'pullup',
                'PSU_MIO_44_DRIVE_STRENGTH': '4',
                'PSU_MIO_44_POLARITY': 'Default',
                'PSU_MIO_44_INPUT_TYPE': 'cmos',
                'PSU_MIO_44_SLEW': 'slow',
                'PSU_MIO_44_DIRECTION': 'inout',
                'PSU_MIO_45_PULLUPDOWN': 'pullup',
                'PSU_MIO_45_DRIVE_STRENGTH': '12',
                'PSU_MIO_45_POLARITY': 'Default',
                'PSU_MIO_45_INPUT_TYPE': 'cmos',
                'PSU_MIO_45_SLEW': 'fast',
                'PSU_MIO_45_DIRECTION': 'inout',
                'PSU_MIO_46_PULLUPDOWN': 'pullup',
                'PSU_MIO_46_DRIVE_STRENGTH': '4',
                'PSU_MIO_46_POLARITY': 'Default',
                'PSU_MIO_46_INPUT_TYPE': 'cmos',
                'PSU_MIO_46_SLEW': 'slow',
                'PSU_MIO_46_DIRECTION': 'inout',
                'PSU_MIO_47_PULLUPDOWN': 'pullup',
                'PSU_MIO_47_DRIVE_STRENGTH': '4',
                'PSU_MIO_47_POLARITY': 'Default',
                'PSU_MIO_47_INPUT_TYPE': 'cmos',
                'PSU_MIO_47_SLEW': 'slow',
                'PSU_MIO_47_DIRECTION': 'inout',
                'PSU_MIO_48_PULLUPDOWN': 'pullup',
                'PSU_MIO_48_DRIVE_STRENGTH': '4',
                'PSU_MIO_48_POLARITY': 'Default',
                'PSU_MIO_48_INPUT_TYPE': 'cmos',
                'PSU_MIO_48_SLEW': 'slow',
                'PSU_MIO_48_DIRECTION': 'inout',
                'PSU_MIO_49_PULLUPDOWN': 'pullup',
                'PSU_MIO_49_DRIVE_STRENGTH': '4',
                'PSU_MIO_49_POLARITY': 'Default',
                'PSU_MIO_49_INPUT_TYPE': 'cmos',
                'PSU_MIO_49_SLEW': 'slow',
                'PSU_MIO_49_DIRECTION': 'inout',
                'PSU_MIO_50_PULLUPDOWN': 'pullup',
                'PSU_MIO_50_DRIVE_STRENGTH': '4',
                'PSU_MIO_50_POLARITY': 'Default',
                'PSU_MIO_50_INPUT_TYPE': 'cmos',
                'PSU_MIO_50_SLEW': 'slow',
                'PSU_MIO_50_DIRECTION': 'inout',
                'PSU_MIO_51_PULLUPDOWN': 'pullup',
                'PSU_MIO_51_DRIVE_STRENGTH': '4',
                'PSU_MIO_51_POLARITY': 'Default',
                'PSU_MIO_51_INPUT_TYPE': 'cmos',
                'PSU_MIO_51_SLEW': 'slow',
```

```
 'PSU_MIO_51_DIRECTION': 'inout',
 'PSU_MIO_52_PULLUPDOWN': 'pullup',
 'PSU_MIO_52_DRIVE_STRENGTH': '12',
 'PSU_MIO_52_POLARITY': 'Default',
 'PSU_MIO_52_INPUT_TYPE': 'cmos',
 'PSU_MIO_52_SLEW': 'fast',
 'PSU_MIO_52_DIRECTION': '<Select>',
 'PSU_MIO_53_PULLUPDOWN': 'pullup',
 'PSU_MIO_53_DRIVE_STRENGTH': '12',
 'PSU_MIO_53_POLARITY': 'Default',
 'PSU_MIO_53_INPUT_TYPE': 'cmos',
 'PSU_MIO_53_SLEW': 'fast',
 'PSU_MIO_53_DIRECTION': '<Select>',
 'PSU_MIO_54_PULLUPDOWN': 'pullup',
 'PSU_MIO_54_DRIVE_STRENGTH': '4',
 'PSU_MIO_54_POLARITY': 'Default',
 'PSU_MIO_54_INPUT_TYPE': 'cmos',
 'PSU_MIO_54_SLEW': 'slow',
 'PSU_MIO_54_DIRECTION': '<Select>',
 'PSU_MIO_55_PULLUPDOWN': 'pullup',
 'PSU_MIO_55_DRIVE_STRENGTH': '12',
 'PSU_MIO_55_POLARITY': 'Default',
 'PSU_MIO_55_INPUT_TYPE': 'cmos',
 'PSU_MIO_55_SLEW': 'fast',
 'PSU_MIO_55_DIRECTION': '<Select>',
 ...},
'driver': pynq.overlay.DefaultIP,
'device': <pynq.pl_server.embedded_device.EmbeddedDevice at 0xffffb39cfa60>}}
```

The HLS has the default name from the Vivado project of *example_0*.

Check *help* for the HLS IP:

In [21]:
```
ol.example0_0?
```

```
Type:        DefaultIP
String form: <pynq.overlay.DefaultIP object at 0xffff768b6560>
File:        /usr/local/share/pynq-venv/lib/python3.10/site-packages/pynq/overlay.py
Docstring:
Driver for an IP without a more specific driver

This driver wraps an MMIO device and provides a base class
for more specific drivers written later. It also provides
access to GPIO outputs and interrupts inputs via attributes. More specific
drivers should inherit from `DefaultIP` and include a
`bindto` entry containing all of the IP that the driver
should bind to. Subclasses meeting these requirements will
automatically be registered.

Attributes
----------
mmio : pynq.MMIO
    Underlying MMIO driver for the device
_interrupts : dict
    Subset of the PL.interrupt_pins related to this IP
_gpio : dict
    Subset of the PL.gpio_dict related to this IP
```

This tells us that this is not a known IP (type is **DefaultIP**) and will get assigned a default driver in PYNQ. The default driver provides MMIO read/write capability.

Create aliases

Using the labels for the HLS IP and DMA listed above, we can create aliases which will make it easier to write and read the rest of the code in this example.

In [22]:
```
dma = ol.axi_dma_0
dma_send = ol.axi_dma_0.sendchannel
dma_recv = ol.axi_dma_0.recvchannel

hls_ip = ol.example0_0
```

Check the status of the HLS IP

In [23]:
```
hls_ip.register_map
```

Out[23]:
```
RegisterMap {
  CTRL = Register(AP_START=0, AP_DONE=0, AP_IDLE=1, AP_READY=0, RESERVED_1=0, AUTO_RESTART=0, RESERVED_2=0, INTERRUPT
=0, RESERVED_3=0),
  GIER = Register(Enable=0, RESERVED=0),
  IP_IER = Register(CHAN0_INT_EN=0, CHAN1_INT_EN=0, RESERVED_0=0),
  IP_ISR = Register(CHAN0_INT_ST=0, CHAN1_INT_ST=0, RESERVED_0=0)
}
```

Note that the HLS IP is not started yet (AP_START=0). You can also see the IP is *idle* (AP_IDLE=1).

We will start the HLS IP and then start some transfers from the DMA.

We could initiate the DMA transfers first if we preferred. The DMA transfers would *stall* until the IP is started.

Start the HLS IP

We can start the HLS IP by writing 0x81 to the control register. This will set bit 0 (AP_START) to "1" and bit 7 (AUTO_RESTART) to "1". AUTO_RESTART means the IP will run continuously. If we don't set this then after the IP completes one full operation or iteration, it will stop and wait until AP_START is set again. We would have to set this every time we want the IP to process some data.

In [24]:
```
CONTROL_REGISTER = 0x0
hls_ip.write(CONTROL_REGISTER, 0x81) # 0x81 will set bit 0
```

Check the correct bits have been set.

In [25]:
```
hls_ip.register_map
```

Out[25]:
```
RegisterMap {
  CTRL = Register(AP_START=1, AP_DONE=0, AP_IDLE=0, AP_READY=0, RESERVED_1=0, AUTO_RESTART=1, RESERVED_2=0, INTERRUPT
=0, RESERVED_3=0),
  GIER = Register(Enable=0, RESERVED=0),
  IP_IER = Register(CHAN0_INT_EN=0, CHAN1_INT_EN=0, RESERVED_0=0),
  IP_ISR = Register(CHAN0_INT_ST=0, CHAN1_INT_ST=0, RESERVED_0=0)
}
```

DMA send

Now we will send some data from DRAM to the HLS IP. Once the HLS IP is started, the steps are the same as the previous DMA tutorial.

Note the array used below is uint32. This was selected to match the type of data width of the HLS IP and the widths used for the DMA. The DMA will transfer blocks of data and may "reformat" it based on the internal data widths in the hardware. The array we create in the notebook effects how the data is formatted in Python. This is an area that can cause problems so it is worthwhile checking you understand your data formats and data movement in your hardware. If you see the wrong

In [26]:
```
from pynq import allocate
import numpy as np

data_size = 100
input_buffer = allocate(shape=(data_size,), dtype=np.int_)
```

Initialize the array.

In [27]:
```
for i in range(data_size):
    input_buffer[i] = i+100
```

Start the DMA transfer

In [28]:
```
dma_send.transfer(input_buffer)
```

DMA receive

Readback data from the HLS IP and store in DRAM. Start by creating the output buffer

In [29]:
```
output_buffer = allocate(shape=(data_size,), dtype=np.uint32)
```

In [30]:
```
dma_recv.transfer(output_buffer)
```

Print first few values of buffer

The result from the HLS IP should be "i"+5

In [31]:
```
for i in range(10):
    print('0x' + format(output_buffer[i], '02x'))
```

```
0x69
0x05
0x6a
0x05
0x6b
0x05
0x6c
0x05
0x6d
0x05
```

In [32]:
```
# Send more data to DMA
```

```
for i in range(data_size):
    input_buffer[i] = i+10



dma_send.transfer(input_buffer)
dma_recv.transfer(output_buffer)
for i in range(10):
    print('0x' + format(output_buffer[i], '02x'))
```

```
---------------------------------------------------------------------------
RuntimeError                              Traceback (most recent call last)
Input In [32], in <cell line: 9>()
      4 for i in range(data_size):
      5     input_buffer[i] = i+10
----> 9 dma_send.transfer(input_buffer)
     10 dma_recv.transfer(output_buffer)
     11 for i in range(10):

File /usr/local/share/pynq-venv/lib/python3.10/site-packages/pynq/lib/dma.py:136, in _SDMAChannel.transfer(self, array, start, nbytes)
    107 """Transfer memory with the DMA
    108
    109 Transfer must only be called when the channel is idle.
   (...)
    133
    134 """
    135 if not self.running:
--> 136     raise RuntimeError("DMA channel not started")
    137 if not self.idle and not self._first_transfer:
    138     raise RuntimeError("DMA channel not idle")

RuntimeError: DMA channel not started
```

Verify that the arrays are equal

In [33]:
```
print("Arrays are equal: {}".format(np.array_equal(input_buffer, output_buffer-5)))
```

```
Arrays are equal: False
```

Free all the memory buffers

Don't forget to free the memory buffers to avoid memory leaks!

In [34]:
```
del input_buffer, output_buffer
```

Summary

In this tutorial you saw how to create a HLS IP with AXI Streams, incorporate this IP into a Vivado design and connected the AXI streams to a DMA, and how to use the HLS IP from PYNQ. The HLS design was very simple, incrementing the input value and writing it to the output. You should be able to see how you can create more advanced HLS kernels. You can also have multiple AXI stream interfaces in your HLS kernel by adding more input or output parameters.

The AXI DMA used in this design supports one AXI stream input and/or one AXI output stream. You can use multiple DMAs if you need to send data to additional AXI stream interfaces.

In [ ]: